REMARKS

This paper is being provided in response to the Final Office Action mailed July 23, 2003, for the above-referenced application. In this response, Applicant has amended claims 1 and 6 to clarify that which Applicant considers to be the invention. Applicant respectfully submits that the amendments to the claims are fully supported by the originally-filed specification.

The rejection of claims 1-11 and 20-23 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement has been addressed by amendments to the claims contained herein according to the guidelines set forth in the Office Action. Applicant respectfully submits that claims 1-11 and 20-23, as amended, are fully supported by the specification. (See, for example, page 9, lines 11 -21; page 12, lines 1-8; and Figures 3 and 4 of the present application). Accordingly, Applicant respectfully requests that this rejection be withdrawn.

The rejection of claims 1-11 and 20-23 under 35 U.S.C. 112, second paragraph, as being indefinite has been addressed by amendments to the claims contained herein according to the guidelines set forth in the Office Action. Independent claims 1 and 6 have been amended to recite that the sidewall offset is an element connected to the sidewall and thus make clear the feature that the *sidewall offset* extends by an amount that is greater than a thickness of the *sidewall*. Accordingly, Applicant respectfully requests that this rejection be withdrawn.

The rejection of claims 1, 3-6, 9-11, 20 and 22 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,439,835 to Gonzalez (hereinafter "Gonzalez") in view of

U.S. Patent No. 5,545,575 to Cheng et al. (hereinafter "Cheng") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Applicant's claim 1, as amended herein, recites a semiconductor device including a semiconductor substrate, an insulating film formed at a surface of the semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated, and a gate electrode formed on the semiconductor substrate, the gate electrode and the insulating film defining lightly doped first drain and source diffusion layers. There are second drain and source diffusion layers surrounding the first drain and source electrodes and aligned to the sidewall. The sidewall has a horizontal offset extending by more than the vertical thickness of the lateral portion of the sidewall. Further, the lightly doped first drain and source diffusion layers extend towards the gate electrode beyond an edge of the sidewall offset, and the heavily doped second drain and source diffusion layers extend below said sidewall offset but are spaced outwardly away from an edge of the gate electrode in a direction along said horizontal surface of said semiconductor substrate. Claims 2-5, 20 and 21 depend directly or indirectly on independent claim 1 and recite additional patentable features thereto.

Applicant's claim 6, as amended herein, recites a semiconductor device including a semiconductor substrate, an insulating film formed at a surface of the semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated, and a gate electrode formed on the semiconductor substrate, the gate electrode and the insulating film defining lightly doped first drain and source diffusion layers. There is at least one sidewall

covering the gate electrode, and heavily doped second drain and source diffusion layers formed at a surface of the semiconductor substrate around the gate electrode and aligned with the sidewall covering, with the first drain and source diffusion layers surrounding the second drain and source diffusion layers on at least a bottom and four lateral sides. The sidewall has a sidewall offset extending outwardly of the gate electrode along a horizontal surface of the semiconductor substrate in at least one region below which at least one of the second drain and source diffusion layers are formed. The sidewall offset extends along a lateral surface of the gate oxide film on which the gate electrode is formed by an amount that is greater than the vertical thickness of the lateral surface of the sidewall, and there are low-resistive wiring layers formed at the surface of the drain and source diffusion layers, located outwardly beyond a peripheral edge of the sidewall and offset in at least one drain and source diffusion layer. Further, the lightly doped first drain and source diffusion layers extend towards the gate electrode beyond an edge of the sidewall offset, and the heavily doped second drain and source diffusion layers extend below said sidewall offset but are spaced outwardly away from an edge of the gate electrode in a direction along said horizontal surface of said semiconductor substrate. Claims 7-11, 22 and 23 depend directly or indirectly on independent claim 6 and recite additional patentable features thereto.

The Gonzalez reference discloses a process for fabricating a CMOS DRAM using a high energy ion implantation of boron ions at a oblique angle for punch through protection. The graded junction 24B is formed by the oblique implantation. The junction of the diffusion is not aligned to the edge of the sidewall offset over gates 16 and 17. (See Abstract and Figures 8 and 9 of Gonzalez).

The Cheng reference discloses an insulated gate semiconductor device having gate electrodes, and a source region 57 nested inside source region 43, etc. Openings in a layer of dielectric material 63 expose portions of the source/drain diffusion regions to form silicide 64. Cheng is used in the Office Action to show that first source/drain diffusion regions may surround second source/drain diffusion regions and have different diffusion concentrations. (See Abstract; col. 5, lines 39-67; and Figure 7 of Cheng).

Applicant's independent claims, as amended herein, all recite a semiconductor device having at least the feature of *said lightly doped first drain and source diffusion layers extending towards said gate electrode beyond an edge of said sidewall offset, and said heavily doped second drain and source diffusion layers extending below said sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said horizontal surface of said semiconductor substrate.* This structure makes it possible for the source and drain diffusion layers, by being outwardly spaced away from the edge of the gate electrode of a transistor, to have a high breakdown voltage thereby preventing generation of a leakage current between bands. (See, for example, page 9, lines 11 -21; page 12, lines 1-8; and Figures 3 and 4 of the present application).

Applicant respectfully submits that neither Gonzalez nor Cheng, taken alone or in any combination, teach or suggest at least the above features as claimed by Applicant. Specifically, Gonzalez discloses a gate electrode, sidewall and sidewall offset and drain and source regions (see, for example, Figure 9 of Gonzalez), but does not disclose heavily doped second drain and

source regions extending below the sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said horizontal surface of said semiconductor substrate. Gonzalez does not show, in any of the figures, multiple drain and source diffusion layers below a region having a sidewall and a sidewall offset connected thereto. The multiple drain and source diffusion layers shown by Gonzalez are shown between gate electrodes 16 and not on the side of the gate electrodes having the sidewall and sidewall offset as is described and claimed by Applicant.

Applicants respectfully submit that Cheng does not overcome the above-noted deficiencies of Gonzalez with respect to Applicant's claims. Cheng discloses a polysilicon plug 28 to which is attached gate electrode extension material portions 49 and 52 and first and second dopant regions 43, 44 and 57, 58. (See col. 5, lines 39-67 of Cheng). Cheng's dopant regions 57 and 58 extend below so as to overlap vertically with the gate electrode portions 49 and 52 such that these regions are NOT *outwardly spaced away from an edge of the gate electrode in a direction corresponding to the horizontal surface of said semiconductor substrate.* Applicant, on the other hand, describes and recites that heavily doped second drain and source extend below the sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said horizontal surface of said semiconductor substrate, and has found that such a structure enhances the breakdown voltage of a transistor.

Applicant respectfully submits that neither Gonzalez nor Cheng, taken alone or in any combination, teach or fairly suggest a semiconductor device having *said lightly doped first drain and source diffusion layers extending towards said gate electrode beyond an edge of said*

sidewall offset, and said heavily doped second drain and source diffusion layers extending below said sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said horizontal surface of said semiconductor substrate, as is claimed by Applicant. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claim 7 under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Cheng and further in view of U.S. Patent No. 5,316,977 to Kunishima et al. (hereinafter "Kunishima") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Claim 7 depends from independent claim 6, discussed above, and recites that low-resistive wiring layers are composed of TiSi.

The Gonzalez and Cheng references are discussed above.

The Kunishima reference is cited by the Office Action as disclosing a silicide layer comprising titanium silicide, using a semiconductor device as a CMOS device, and a sidewall entirely covering the gate electrode.

Applicant respectfully submits that Kunishima fails to overcome the above-noted deficiencies of the Gonzalez and Cheng references. Applicant respectfully submits that neither Kunishima, Gonzalez nor Cheng, taken alone or in any combination, teach or fairly suggest a semiconductor device having *said lightly doped first drain and source diffusion layers extending*

towards said gate electrode beyond an edge of said sidewall offset, and said heavily doped second drain and source diffusion layers extending below said sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said horizontal surface of said semiconductor substrate, as is claimed by Applicant. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 1-4, 8-10, 21 and 23 under 35 U.S.C. 103(a) as being unpatentable over Cheng is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Claims 2-3, 8-10, 21 and 23 depend on independent claims 1 and 6, discussed above, and recite additional patentable features thereto.

The Cheng reference is discussed above with respect to Applicant's claims. As noted, Applicant respectfully submits that Chang does not teach or fairly suggest a semiconductor device having *said lightly doped first drain and source diffusion layers extending towards said gate electrode beyond an edge of said sidewall offset, and said heavily doped second drain and source diffusion layers extending below said sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said horizontal surface of said semiconductor substrate*, as is claimed by Applicant. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 5, 7, 11, 21 and 23 under 35 U.S.C. 103(a) as being unpatentable over Cheng in view of Kunishima is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Claims 5, 7, 11, 21 and 23 depend on independent claims 1 and 6, discussed above, and recite additional patentable features thereto.

The Cheng and Kunishima references are discussed above.

Applicant respectfully submits that neither Chang nor Kunishima, taken alone or in any combination, teach or fairly suggest a semiconductor device having *said lightly doped first drain and source diffusion layers extending towards said gate electrode beyond an edge of said sidewall offset, and said heavily doped second drain and source diffusion layers extending below said sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said horizontal surface of said semiconductor substrate,* as is claimed by Applicant. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
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